Claims:

1. An SDH transmission apparatus, characterized in that it comprises:

a plurality of interface units (2) for accommodating main signal frames including channel data of a plurality of channels and compliant with an SDH transmission system; and

a main signal processing unit (3A) accommodating said interface units (2) for performing predetermined main signal processing for the main signal frames; that

said main signal processing unit (3A) includes

a frame timing production section (32-9) for producing an intra-apparatus reference frame timing based on an intra-apparatus reference clock;

a frame timing distribution section (32-9) for distributing the intra-apparatus reference frame timing produced by said frame timing production section to said interface units; and

a main signal timing re-clocking section (32-2) for synchronizing frame timings of the main signal frames with the intra-frame reference frame timing using a main signal memory section (32A) for temporarily storing the main signal frames; and that

each of said interface units (2) includes

a main signal signaling processing section (21) for performing signaling processing of a main signal frame

to said main signal processing unit based on the intra-apparatus reference frame timing distributed from said frame timing distribution section (32-9) of said main signal processing unit.

2. An SDH transmission apparatus as set forth in claim 1, characterized in that said main signal processing unit (3A) includes

a cross connect section (32) for performing cross connect processing in a unit of channel data for the main signal frames from said main signal timing re-clocking section (33-2).

3. An SDH transmission apparatus as set forth in claim 1, characterized in that

each of said interface units (2) includes

a frame synchronizing signal application section (21-2) for applying a frame synchronizing signal to a main signal frame, and

said main signal processing unit (3A) includes, for each of said interface units (2),

a frame synchronizing section (32-1) for detecting the frame synchronizing signal from the main signal frame from the interface unit (2) to establish synchronism of the main signal frame.

4. An SDH transmission apparatus as set forth in claim

1, characterized in that

each of said interface units (2) includes

a first transmission rate conversion section (22-1) for converting the rate of a main signal frame into a predetermined inter-unit transmission rate and transmitting the resulting main signal frame to said main signal processing unit, and

said main signal processing unit (3A) includes, for each of said interface units (2),

a second transmission rate conversion section (31-1) for converting the rate of a main signal frame from said first transmission rate conversion section (22-1) of any of said interface units (2) into the predetermined intra-apparatus transmission rate.

5. An SDH transmission apparatus as set forth in claim 4, characterized in that said main signal processing unit (3A) includes

a main PLL circuit (34) for performing PLL processing for the intra-apparatus reference clock, and

a sub PLL circuit (31-2) provided for each of the second transmission rate conversion sections (31-1) for performing PLL processing for the intra-apparatus reference clock after the PLL processing by said main PLL circuit (34) and supplying the resulting intra-apparatus reference clock as an operation clock for the second transmission rate conversion section (31-1).

6. An SDH transmission apparatus as set forth in claim 5, characterized in that said main PLL circuit (34) includes

a distribution outputting section (34-9) for outputting the intra-apparatus reference clock after the PLL processing individually for the sub PLL circuits (31-2).

7. An SDH transmission apparatus as set forth in claim 5, characterized in that

at least one of the sub PLL circuits (31-2) produces a master clock of an intra-apparatus reference based on the intra-apparatus reference clock, and

said main signal processing unit (3A) includes

a frame timing re-clocking section (32-10) for synchronizing the intra-apparatus reference frame timing produced by said frame timing production section with the master clock.

8. An SDH transmission apparatus as set forth in claim 1, characterized in that,

where said main signal processing unit has a redundancy configuration including an work main signal processing unit (3A) and a protection main signal processing unit (3B), and

each of said main signal processing units (3A and 3B) includes

a reference clock selection section (32-8) for

selecting a normal one of the intra-apparatus reference clocks of said work and protection main signal processing units.

9. An SDH transmission apparatus as set forth in claim 8, characterized in that each of said main signal processing units (3A and 3B) includes

a clock selection setting interface section (32-11) for performing setting for clock selection of said reference clock selection section in accordance with an external clock selection instruction.

10. An SDH transmission apparatus as set forth in claim 1, characterized in that,

where said main signal processing unit has a redundancy configuration including an work main signal processing unit (3A) and a protection main signal processing unit (3B), and

each of said main signal processing units (3A and 3B)

mutually transfer intra-unit synchronizing timings based on the intra-apparatus reference clocks to synchronize intra-apparatus reference frame timings thereof with each other.

11. An SDH transmission apparatus as set forth in claim 10, characterized in that

said frame timing production section (32-9) of the work main signal processing unit (3A) includes

a first counter section (53) for performing a predetermined counting operation to produce the inter-unit synchronizing timing, and

said frame timing production section (32-9) of said protection main signal processing unit (3B) includes

a clock phase protection section (51) for performing clock phase protection for the inter-unit synchronizing timing produced by said first counter section (53) and re-clocking the inter-unit synchronizing timing to a frame timing synchronized with the inter-unit reference frame timing of said work main signal processing unit based on the intra-frame reference clock,

a frame phase protection section (52) for performing frame phase protection for the frame timing from said clock phase protection section (51), and

a second counter section (53) for performing a predetermined counting operation based on the frame timing after the frame phase protection by said frame phase protection section to produce an intra-apparatus reference frame timing for said protection main signal processing unit itself.

12. An SDH transmission apparatus as set forth in claim 11, characterized in that said clock phase protection section (51) includes:

a first memory section (51A) for storing the inter-unit synchronizing timing and reading out the inter-unit synchronizing timing based on the intra-apparatus reference clock to synchronize the inter-unit synchronizing timing with the intra-apparatus reference frame timing;

a first frame timing production counter section (51E) for performing a predetermined counting operation based on the inter-unit synchronizing timing read out from said first memory section (51A) to produce the frame timing synchronized with the intra-frame reference frame timing; and

a first phase difference correction control section (51D) for detecting a phase difference of the inter-unit synchronizing timing before and after the inter-unit synchronizing timing passes said first memory section (51A) and performing correction control of the counting operation of said first frame timing production counter section (51E) so that the phase difference may be reduced to zero.

13. An SDH transmission apparatus as set forth in claim 7, characterized in that said frame timing re-clocking section (32-10) includes:

a second memory section (81) for storing the intra-apparatus reference frame timing produced by said frame timing production section and reading out the

intra-apparatus reference frame timing based on the master clock to synchronize the intra-apparatus reference frame timing with the master clock;

a second frame timing production counter section (85) for performing a predetermined counting operation based on the intra-apparatus reference frame timing read out from said second memory section (81) to produce the intra-apparatus reference frame timing synchronized with the master clock; and

a second phase difference correction control section (84) for detecting a phase difference of the inter-unit reference frame timing before and after the inter-unit reference frame timing passes said second memory section (81) and performing correction control of the counting operation of said second frame timing production counter section (85) so that the phase difference may be reduced to zero.

14. An SDH transmission apparatus as set forth in claim 4, characterized in that each of said interface units (2) includes

a first transmission rate conversion setting interface section (24) for performing setting for transmission rate conversion of said first transmission rate conversion section (22-1) in accordance with an external transmission rate setting.

15. An SDH transmission apparatus as set forth in claim

4, characterized in that said main signal processing unit (3A) includes

a second transmission rate conversion setting interface section (32-11) for performing setting for transmission rate conversion of said second transmission rate conversion section (31-1) in accordance with an external transmission rate setting.

16. A frame timing re-clocking method for an SDH transmission apparatus which accommodates main signal frames of a plurality of channels compliant with an SDH transmission system, characterized in that

a frame timing of a received main signal frame is re-clocked to an intra-apparatus reference frame timing without using pointer processing to establish synchronism.